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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	08/816,891	OTA ET AL.	
	Examiner	Art Unit	
	Leonid Shapiro	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-22 and 34* is/are rejected.

7)☒ Claim(s) *23-33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 17-22 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuo et al (U.S. Patent No. 5,666,133; hereinafter simply referred to as Matsuo) in view of Kimura et al (U. S. Patent No. 5,253,091; hereinafter briefly referred to as Kimura).

As to claim 17, Matsuo discloses a matrix panel display apparatus including plural signal lines (9) and plural scanning lines (10) intersecting each other, and near intersection point, a picture element (7) including a picture element electrode (5), a counter electrode (11), a display medium (liquid crystal) disposed between the picture element electrode (5) and counter electrode (7) and a transistor (4) for applying image signals (Vs). Matsuo teaches a plurality of storage capacitances (8), each connected to a respect to one of picture elements (7). Matsuo teaches a picture signal generating means (2) for dividing plural picture elements (7) into two groups (i.e. a plurality of columns or groups are formed by column conductors 9). Matsuo teaches that the image signal Vs is inverted in polarity every one horizontal scanning period as well as every cycle; see column 1, line 63 through column 2, line 23 and column 6, lines 17-21. Thus, Matsuo clearly teaches the image signal (Vs) applied to a first group or a first column

being inverted form of the image signal applied to the signal line of a second column or second group.

Matsuo teaches that the counter electrode signal (Vt) is a signal applied to the counter electrode as periodically inverted in polarity in synchronization with inversion in polarity of the image signal Vs; see column 6, lines 22-30 and see figure 4, waveform Vt and Vs(m). This reads on the claimed "bias signal generating means" as recited in the claim. Matsuo does not mention the plural picture elements selected at the same time by the picture signal generating means. In the same field of endeavor, Kimura teaches that all the TFT's connected to a row which is driven are turned ON. The first data signal Vdm and Vdm+I are simultaneously applied to the column conductors D1 and D2, respectively during a frame cycle T; see figure 5a-5c and see column 3, lines. Thus, Kimura clearly teaches plural picture element selected at the same time in the picture signal generating means (2-3). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the teaching of selecting plural picture elements at the same time by simultaneously applying the data signal to the column conductors as taught by Kimura to the picture signal generating means of Matsuo so as to reduce screen flicker; see column 4, lines 34-41 of Kimura.

As to claim 34, this claim differs from claim 17 in that claim 34 is method whereas claim 17 is apparatus. Thus claim 34 is analyzed as previously discussed with respect to claim 17.

As to claim 18, Matsuo clearly teaches display medium being liquid crystal ; see column 4, lines 59-60.

As to claim 19, both Matsuo and Kimura teach the polarity of image signals reversed in successive frames. For example, figure 5b and 5c of Kimura clearly show the claimed limitation reversed in successive frames.

As to claim 20, since the pixels of Matsuo and Kimura are arranged in a matrix of rows and columns. Thus the number ofpixels in one column or first group is equal to the number of pixels in another column or second group.

As to claim 21, the limitation "every n column elements is alternately assigned to the first group of picture elements and the second group of picture elements, respectively" reads on odd columns and even columns as taught by Kimura and Matsuo.

As to claim 22, Matsuo clearly teaches transistor (4) having three terminals, first terminal is connected to scanning line (10), second terminal is connected to signal line (9) and third terminal is connected to picture element electrode (5) and storage capacitor (Cvc). Matsuo clearly teaches the limitation two group bias signals (Vt) applied to storage capacitor (Cvc).

Allowable Subject Matter

3. Claims 23-33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Relative to claim 23 the major difference between the teaching of the prior art of

record (Matsuo and Kimura) and the instant invention is that wherein said bias signal generating circuit includes scanning signal generating circuit for applying a scanning voltage to said picture elements through said scanning lines.

Relative to claim 24 the major difference between the teaching of the prior art of record (Matsuo and Kimura) and the instant invention is that wherein a terminal of a storage capacitance belonging to said first group of picture elements is connected to a scanning line which is located one line before a line being scanned presently; wherein a terminal of a storage capacitance belonging to said second group of picture elements is connected to a scanning line which is located one lin~ behind a line being scanned presently; wherein said bias signal generating means operates to apply a first bias signal to a scanning line which is located one line before a line being scanned presently and to apply a second bias signal of the polarity reverse to said first bias signal to a scanning line which is located one line behind a line being scanned presently, while one scanning line is selected; and wherein said apparatus further [including] comprises an image signal generating circuit which applies image signals having a polarity reverse to said first bias signal to said first group of picture elements and image signals having the polarity reverse to said second bias signal to said second group of picture elements.

Claims 25-33 depend on claim 24.

Telephone Inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LS
05.24.07

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